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HIGHLY INTEGRATED GaAs MMIC RF FRONT END FOR PCMCIA PCS APPLICATIONS

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Abstract

A fully integrated GaAs Microwave Monolithic Integrated Circuits (MMIC) transceiver chip for use on Personal Computer Memory Card International Association (PCMCIA) card in wireless modem and Local Area Network (LAN) aplications is described. The chip is small in size ($100x150mil^2$) and exhibits good performance after the first fabrication pass. An ongoing activity to further improve the electrical performance, reduce the size of the chip and develop a low cost composite package using multilayer ceramic microwave integrated circuits (MCMIC) is also outlined. A proposed system-specification and -architecture is presented.

1. Introduction

This paper describes the design, fabrication, and performance of a highly integrated GaAs MMIC radio frequency (RF) front-end. Designed specifically for wireless modem and LAN applications, the front-end achieves the performance and small size necessary to contain all RF and digital hardware on a single PCMCIA card. Such cards are increasingly used to expand the capabilities of notebook and palm-size computers.

The RF front-end employs a highly integrated transceiver chip. The GaAs Integrated Circuit (IC) includes an upconverter, a medium-power output amplifier, a transmit/receive switch, a low-noise input amplifier, and a downconverter. A Voltage Controlled Oscillator (VCO) is also included on the PCS transceiver chip to supply an LO signal to both the upconverter and the downconverter. The chip is designed to operate from 800 to 1800 MHz.

The Personal Communication System (PCS) transceiver IC described exhibits good performance after first-pass fabrication. The front-end utilizes the MMIC on a MCMIC substrate. This approach should significantly reduce the size of the front end. MCMIC will include a synthesizer IC for the transceiver LO, as well as biasing and filtering components not included on the transceiver chip.

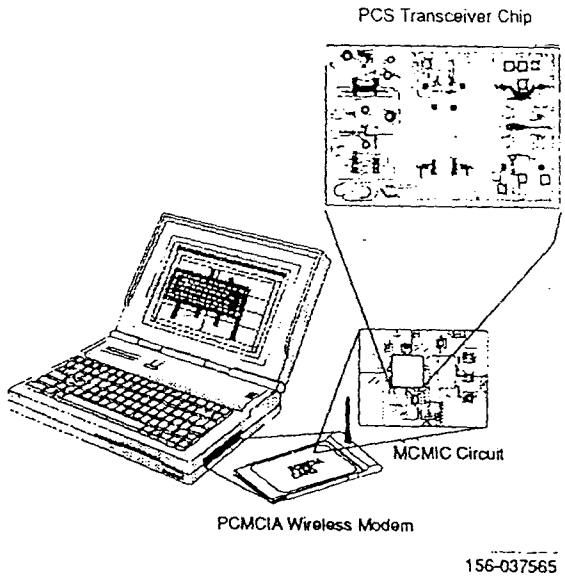

Figure 2-1. Wireless data communications using highly integrated PCS MMIC chip.

2. Applications

The transceiver MMIC demonstrates the highly integrated GaAs MMIC subsystem development capabilities of the Advanced Microwave Technology group at Northrop Electronic Systems Division (Rolling Meadows, IL). The technology under development is suitable for a variety of commercial applications, including PCS and Intelligent Vehicular Highway Systems (IVHS), and also for military Electronic Warfare (EW) systems.

The great demand for portable phones during recent years is expected to continue, as more wireless modem and LAN products are offered to the public. One such wireless data communication device, that is being developed at ESD-RMS, is illustrated in Figure 2-1.

3. GaAs MMIC PCS Chip

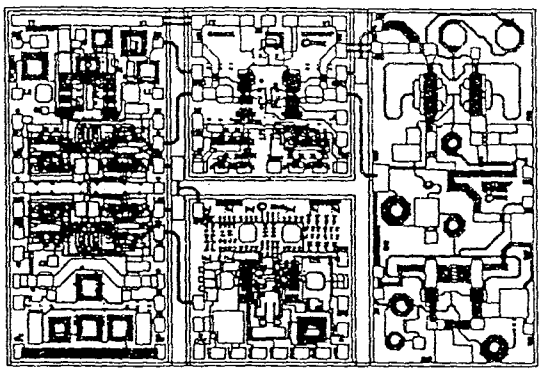

Figure 3-1. Transceiver MMIC with all RF functions for wireless LAN/modem.

The transceiver MMIC (Figure 3-1) is a fully integrated chip on a GaAs-substrate. It measures 100 x 150 mil^2 . The chip is designed to cover the bandwidth 0.8-1.8 GHz. It has all the essential RF functional blocks (Figure 3-2) for a transmit/receive (T/R) RF front end in wireless modem/LAN and cellular applications. In this section the functional blocks will be discussed, and measured data will be presented for individual blocks. The measured data were taken after the first pass fabrication of the chip. The chip is being slightly redesigned to accommodate additional functions and to reduce the size by 33%. The final chip size will be 100 x 100 mil^2. The main advantages of a higher level of integration are smaller size, lower cost, high reliability and ease of assembly.

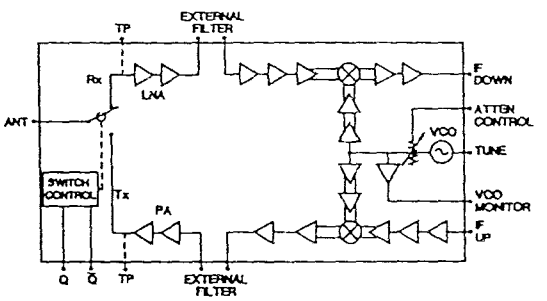

Figure 3-2. Essential RF functional blocks on transceiver chip.

The receive path of the transceiver chip (Figures 3-1 and 3-2) consists of two stages of low noise amplification, followed by an external filter (optional), a differential down converter and two stages of intermediate frequency (IF) amplification. The transmit path has three stages of IF amplification followed by differential up-conversion and two stages of power amplification. The transmit/receive (T/R) switch at the output routes transmit and receive signals to and from the antenna, respectively.

The individual building blocks of the integrated PCS chip have been characterized and the performance data are shown below. The whole PCS chip is being mounted in a package for full charaterization as an integrated chip.

Description and Performance of Individual MMIC in the Transceiver Chip

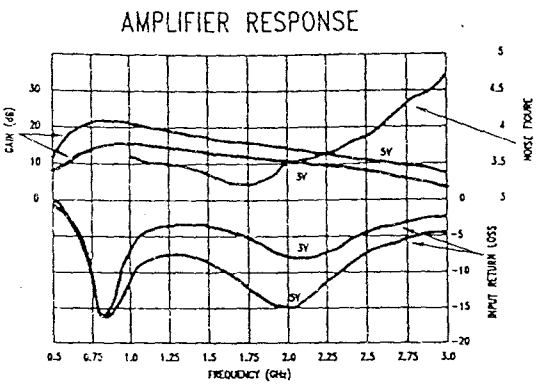

Figure 3-3. Gain, Noise Figure and Return loss of the LNA in the transceiver chip.

Low Noise Amplifier (LNA): The LNA has two stages of amplification and is designed to operate from 0.8 to 2.4 GHz. It operates from a single positive supply (3-5V) with low power dissipation (30-50 mW). The active devices are enhancement metal semiconductor field effect transistors (MESFETs). Resistive biasing is used and it decreases the size of the chip at a slight cost of dissipated power and reduced efficiency. In the receive path, the total current drawn from the supply by the LNA is 10-12 mA. The MESFETs, after the resistive drop in the drain bias circuits operate very close to the knee voltage of the I-V curves. The measured performance of the LNA is shown in Figure 3-3. The performance is shown at both VD=3V and 5V. At VD=5V, the amplifier shows a gain of 20 dB from 0.8 to 1.25 GHz and it rolls off to 12 dB at 2.6 GHz. At VD=3V, the gain is between 10 and 15 dB over most of the 0.8-2.4GHz band.

The noise figure is less than 3.5 dB over this same 0.8-2.4 GHz bandwidth. The chip is redesigned for the second iteration to deliver a gain of 20 dB at VD=5V and a noise figure of 3 dB from 0.8 to 2.4 GHz.

Down-, Up-Converter: The converter MMICs form a part of a bigger section in the transceiver chip that also has the LNA and a 90° splitter. The 90° splitter is not being used on this iteration. The splitter will be added on the second iteration to provide I-Q outputs.

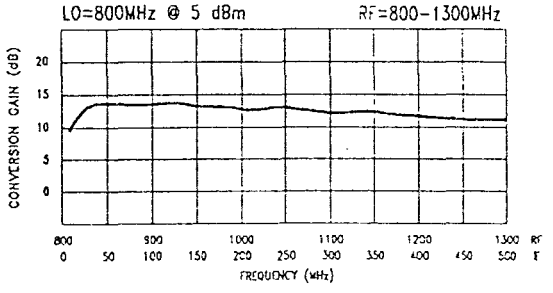

Figure 3-4. Performance of the down-converter in the transceiver chip.

The RF is first amplified by a two stage amplifier and then split by a differential amplifier for feeding to a MESFET-quad mixer. The LO is also split and amplified by a two stage differential amplifier and then fed to the gates of the FET-quad mixer. The IF from the FET-quad mixer is combined and amplified through a differential amplifier to provide single ended output.

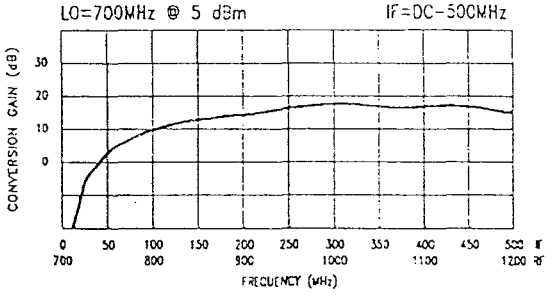

Figure 3-5. Performance of the up-converter in the transceiver chip.

The dc power consumption of the converter is approximately 100 mW for a 5V drain supply. Figure 3-4 shows the down conversion gain with the LO fixed and RF varied. Up to 1300 MHz, the conversion gain is 11-12 dB. Figure 3-5 similarly shows the up-conversion performance. The up-converter is a mirror image of the down-converter along the X-axis. The up-conversion performance degrades at lower IF (less than 100 MHz). Above 100 MHz IF, the up-conversion gain is more than 10 dB.

In the second iteration, the up-conversion gain is being increased to more than 10 dB for an IF down to 30 MHz, by increasing the coupling capacitor between IF amplifier stages.

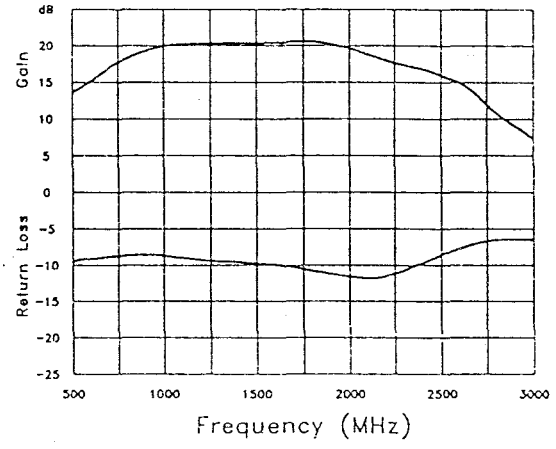

Figure 3-6. Small signal response of the power amplifier in the transceiver chip.

Power Amplifier: The power amplifier in the transmit path is designed to deliver 25-27 dBm of power at 1-3 dB compression points with 18-20 dB of gain over 0.8-1.8 GHz. It uses off-chip coils and capacitors for dc-biasing. The off-chip bias components are necessary to handle the total current (350-450 mA). The on-chip coils have low Qs and dissipate a fair amount of dc-power, thus degrading the efficiency. The MMIC occupies 50 x 100 mil^2. The MMIC does not utilize via holes, the ground is provided by a number of bond wires that connect the ground pads (distributed around the chip) to the carrier plate. The MMIC requires a negative gate supply. A self-biasing scheme can be adopted by connecting a resistor and by-pass capacitor to the ground pad. The self-biasing scheme requires a single bias supply at a cost of degraded efficiency. Figure 3-6 shows the small signal response of the power amplifier. The amplifier shows 17-20 dB gain from 0.8 to 2.0 GHz. Figure 3-7 shows the power output and power added efficiency over frequency. The output power at 1 dB compression is more than 25 dBm from 0.8 to 2.0 GHz. The output power is 25-27 dBm for 1-3 dB compresssion or expansion. The associated power added

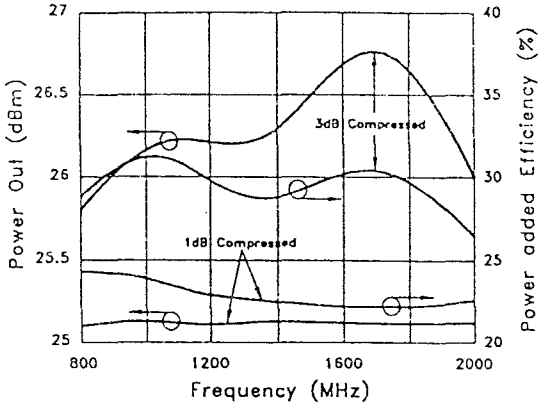

Figure 3-7. Power output and power added efficiency of the power amplifier @P_{1db} and @P_{3db} in the transceiver chip.

efficiencies are between 22 and 30% over the 0.8-2.0 GHz bandwidth. The power output in the second iteration design is being increased to 27 dBm (at 1dB compression point) over the 0.8-2.0 GHz bandwidth.

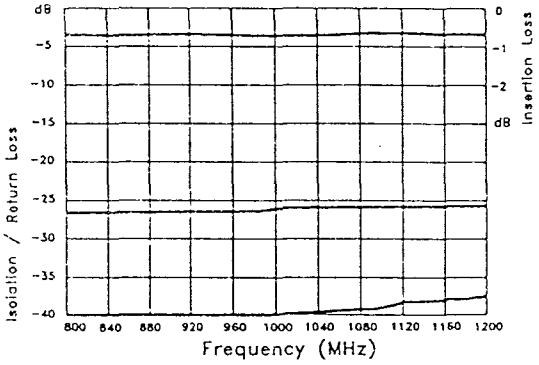

Figure 3-8. Insertion loss, return loss and isolation of T/R switch in the transceiver chip.

Transmit/Receive (T/R) Switch: The T/R switch is a single-pole double-throw (SPDT) type. It routes the signal between the antenna and receiver or transmitter. Its measured performance is shown in Figure 3-8. The switch has an insertion loss of less than 1dB, input output return loss of better than -20dB and an isolation better than 35 dB up to 1.2 GHz. The switch has a 1dB compression point of 24 dBm. In the second iteration, the switch power handling is being increased to 25 dBm and the isolation is being improved to 45 dB.

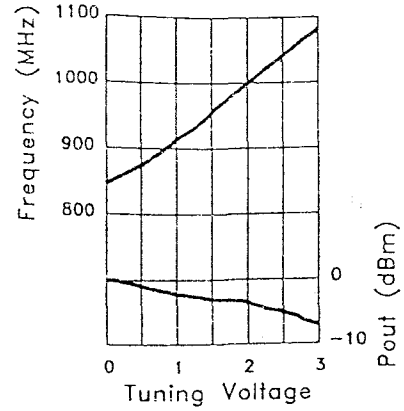

Figure 3-9. Frequency tunability and power output of VCO in the PCS MMIC.

Voltage-Controlled Oscillator (VCO): The on-chip VCO provides the LO for both receive and transmit paths. Tuning is achieved by an off-chip varactor, the capacitance of which is changed by a tuning voltage. The VCO chip also incorporates a buffer amplifier that follows the oscillator. There is an on-chip attenuator (optional) between the oscillator and the buffer amplifier to control the output power. The oscillator and buffer amplifier are designed to draw a total dc current of 18-22 mA from a 3-5V supply. Figure 3-9 presents the measured VCO performance over 0-3V tuning voltage. Total tunability is 840 MHz to 1085 MHz. The power out is 0 to -8 dBm. A redesign of the VCO for the second iteration is underway to increase the power to 6 dBm and tunability from 0.8 to 2.0 GHz range.

Integrated PCS MMIC: The PCS chip is being put in a package as shown in Figure 3-10. The overall system performance as an integrated PCS chip is being evaluated.

4. Example System Architecture

The application for this design is in a PCMCIA card. The product would be housed in a PCMCIA card that plugs into an ExCA compatible port on a portable notebook or handheld computer. There are significant advantages in implementing a wireless data product in a small package. Unrestricted portability is the prime drive of PCMCIA based wireless products. However, along with the smaller package comes the requirement for reduced power consumption. Recent developments in MMIC and MIC

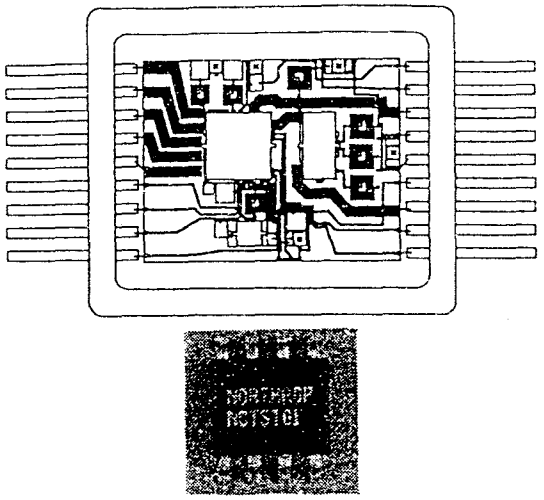

Figure 3-10. The plastic package in which the transceiver MMIC is being inserted along with the multilayer ceramic interfacing circuit.

technologies in the defense industry provide an opportunity to address these requirements.

A proposed modem (Figure 4-1) product would consist of several key functional blocks: 1) PCMCIA interface, 2) digital modem function, 3) spread-spectrum function, 4) RF functional block, and 5) antenna system.

In general, the computer architectures that this wireless modem product will be used with must adhere to the PCMCIA 2.0 standards as well as ExCA interface format compatibility. Most computer manufacturers have adopted these formats as standards for their current and next generation products. The physical form of the module follows along the lines of a Type II extended PCMCIA card. This allows sufficient room to implement the interface, processing, and RF components as well as the antenna system. Due to various host computer physical housing designs, a non-shielded area in the housing for antenna applications cannot be guaranteed. Thus, a small portion of the PCMCIA card may extend out of the host housing.

The system design provides peer-to-peer wireless communications. Such a local wireless network can be used for warehouse inventory-taking, cooperative learning in classrooms, and pen- and notepad-based applications. A peer-to-peer system would consist of two portable computers and two wireless modems. The physical nature of the system is such that its operation would be transparent to the user. Application software and system specific drivers can be easily written to interface with the modem protocols and to provide various specific functions.

PCMCIA Interface: The PCMCIA interface would consist of a 68-pin PCMCIA connector, RAM and ROM, and an interface adapter for communicating card specific functions and configurations to the host computer. The function of the interface follows the card interface structure (CIS) as defined in the PCMCIA 2.0 standard.

Modem Function: The modem function would provide for a maximum of 19.2 Kbps data rates and will interfaces with the host computer through the PCMCIA interface adapter function.

Spread Spectrum Function: The wireless modem would be required to meet FCC part 15 in the 902-928 MHz ISM band for spread-spectrum operation. The spread-spectrum function would be addressed using a PN code generator and matched filter receiver with correlator/accumulator functions. These functions are implemented using the latest in digital signal processing technologies.

RF Function: The RF functional block uses advanced GaAs MMIC device technology as well as advanced MCMIC substrate technology. At the heart of the RF block is the Northrop PCS transceiver chip described earlier. It provides the majority of the RF functions in a 100x100 mil^2 area. These functions include the LNA, downconverter, VCO, upconverter, and .25 watt power amplifier, all operating at a nominal 3-5 volts.

GaAs MMIC provides an enabling technology for high levels of RF subsystem integration. MMICs simplify design and manufacturing for OEMs by reducing package size and weight, reducing parts inventory, and minimizing dependence on skilled technicians all while offering high levels of performance.

Recent technology advances have led to the development of MCMICs which can implement traditional lumped element components in a highly integrated, very dense package. Resistors, capacitors, inductors, and transmission lines are laid out on a ceramic substrate as-off chip circuitry for the GaAs MMIC transceiver chip. The MCMIC circuit provides for a higher level of integration when designed with Northrop MMIC

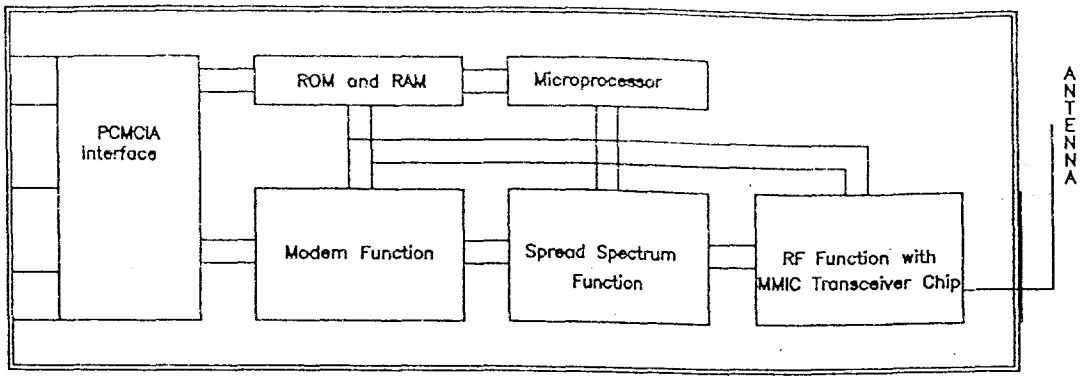

Figure 4-1. Proposed wireless modem PCMCIA card with transceiver chip.

devices.

Due to the high level of integration of the Northrop PCS transceiver MMIC, the RF layout is significantly simplified. All required components can be integrated on the MCMIC substrate as shown early in Figure 3-10. Inductors are realized with planar technology using airbridges and passivated underpasses. Capacitors can be realized with either Metal Insulator Metal (MIM) technology or interdigitated designs. This design uses all MIM capacitors. It should be noted that the MCMIC technology can be used to create a hierarchy where increased levels of integration are made possible by adding more MMIC devices to the design.

Antenna: The internal antenna provides unobstructed working space and easy portability. The design of internal antenna would take into account the PCMCIA card housing in the computer. Other external antennas would not guarantee unobstructed working space, because the location of the external antenna would change as that of PCMCIA card changes on the computer housing.

Modem Specifications: The wireless modem is designed to operate in the 902-928 MHz ISM band at a maximum data transfer rate of 19.2 Kbps. The RF design will adhere to the FCC Part 15 rules for spread spectrum operation with power levels under 1 watt. It would use a bi-phase shift-keyed modulation scheme and incorporate a PN code generator for spectrum spreading providing at least 20 dB of processing gain. The RF spectrum will occupy a 2 MHz bandwidth with a maximum of 13 separate channels. The modem design will meet PCMCIA 2.0 standards and be ExCA compatible.

900 MHz Wireless Modem Specifications

Frequency Band	902-928 MHZ
Maximum Data Transfer Rate:	19.2 Kbps
Power Level:	1 Watt max
Modulation Type:	BPSK
Access Type:	Peer-to-Peer
Module Function:	Wireless Modem
RF Bandwidth:	2 MHz
Number of Channels:	13
Processing Gain:	20 dB

5. Conclusion

A plan and development activities for a highly integrated MMIC transceiver chip for use in a PCMCIA card are presented here. The MMIC chip under development can address other PCS applications including, wireless LAN and cellular phones. The goal is to lower the cost with high volume production and inexpensive packaging. The complete package would use three technologies – plastic, MCMIC and MMIC. The MCMIC technology contains the necessary bias circuits and the interfacing circuit between MMIC and the leads. The projected cost for the complete packaged transceiver is $30 - $40 each by the end of 1995 in volumes of 10,000 or more.

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